IN THE CLAIMS

Please amend claims 1 and 7-12 as follows: 1(Amended). A method for forming a dual damascene structure, comprising: providing a silicon substrate containing one or more electronic devices; forming a first dielectric layer of a first thickness over said silicon substrate; forming a first etch stop layer over said first dielectric layer; forming a second dielectric layer of a second thickness over said first dielectric layer; forming an anti-reflective coating layer over said second dielectric layer; etching a first trench in said second dielectric layer; and			
providing a silicon substrate containing one or more electronic devices; forming a first dielectric layer of a first thickness over said silicon substrate; forming a first etch stop layer over said first dielectric layer; forming a second dielectric layer of a second thickness over said first dielectric layer; forming an anti-reflective coating layer over said second dielectric layer;	Please	e amend claims 1 and 7-12 as follows:	
forming a first dielectric layer of a first thickness over said silicon substrate; forming a first etch stop layer over said first dielectric layer; forming a second dielectric layer of a second thickness over said first dielectric layer; forming an anti-reflective coating layer over said second dielectric layer;	1(Amended). A method for forming a dual damascene structure, comprising:		
forming a first etch stop layer over said first dielectric layer; forming a second dielectric layer of a second thickness over said first dielectric layer; forming an anti-reflective coating layer over said second dielectric layer;		providing a silicon substrate containing one or more electronic devices;	
forming a second dielectric layer of a second thickness over said first dielectric layer; forming an anti-reflective coating layer over said second dielectric layer;		forming a first dielectric layer of a first thickness over said silicon substrate;	
layer; forming an anti-reflective coating layer over said second dielectric layer;		forming a first etch stop layer over said first dielectric layer;	
	layer;	forming a second dielectric layer of a second thickness over said first dielectric	
etching a first trench in said second dielectric layer; and		forming an anti-reflective coating layer over said second dielectric layer;	
		etching a first trench in said second dielectric layer; and	

simultaneously etching a second trench to a first depth in said second dielectric layer and etching said first trench in said first dielectric layer wherein the first depth is approximately equal to the second thickness.

7(Amended). A method for forming a copper filled dual damascene structure, comprising:

providing a silicon substrate containing one or more electronic devices;

forming a first dielectric layer of a first thickness over said silicon substrate;

forming a first etch stop layer over said first dielectric layer;

forming a second dielectric layer of a second thickness over said first dielectric layer;

forming a silicon oxynitride anti-reflective coating layer over said second dielectric layer;

etching a first trench to a first depth in said second dielectric layer and said first dielectric layer wherein the first depth is greater than the thickness of said second dielectric layer; and

simultaneously etching a second trench to a second depth in said second dielectric layer and etching said first trench in said first dielectric layer wherein the second depth is approximately equal to the second thickness.

- 8 (Amended). The method of claim 7 wherein said silicon nitride anti-reflective coating layer comprises 30 to 50 atomic percent of silicon, 20 to 50 atomic percent of oxygen, 2 to 17 atomic percent of nitrogen, and 7 to 35 atomic percent of hydrogen.
- 9 (Amended). The method of claim 7 wherein first and second etch stop layers are formed with material selected from the group consisting of silicon carbide and silicon nitride.
- 10 (Amended). The method of claim 7 wherein said first dielectric layer is FSG.
- 11 (Amended). The method of claim 7 wherein said second dielectric layer is FSG.

12 (Amended). The method of claim 7 further comprising:

forming a liner film in said first trench and said second trench; and

forming a contiguous copper layer in said first trench and said second trench.